VOLUME IV

MODULAR SERIES ON SOLID STATE DEVICES

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Field Effect Devices

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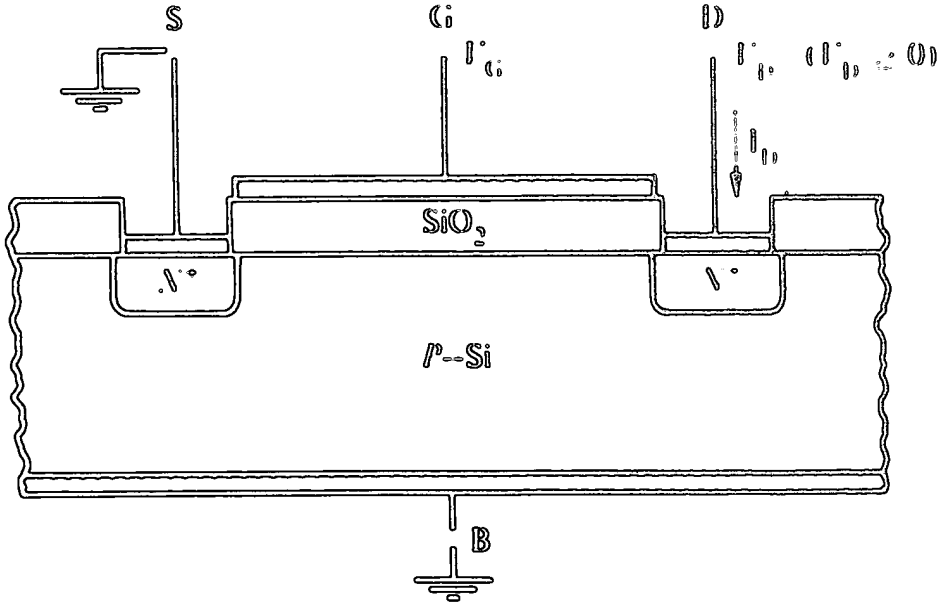

This book is in the
Addison-Wesley Modular Series on Solid State Devices

Library of Congress Cataloging in Publication Data

Pierret, Robert F.
Field effect devices.

(Modular series on solid state devices ; v. 4)
"EE-305."
Bibliography: p.
Includes index.
1. Field-effect transistors. 2. Metal oxide semiconductors.
3. Metal oxide semiconductor — field-effect transistor. I. Title.
II. Series: Pierret, Robert F. Modular series on solid state
devices ; v. 4.
TK 7871.95.P53 621.3815'284 81-15035
ISBN 0-201-05323-3 AACR2

Reprinted with corrections, July 1983

ISBN 0-201-05323-3
HIJKLMNOP-AL-8987

approximation in FET work which was initially introduced and described in the J-FET analysis of Section 1.3.

5.3 THRESHOLD CONSIDERATIONS

Perhaps because of the method of presentation, fledgling device analysts are sometimes under the impression that the nonidealities discussed in relationship to the MOS-C do not affect the MOSFET. This impression is, of course, totally false. Sodium ions in the oxide, for example, can cause the threshold or turn-on voltage for both n- and p-channel devices to occur at large negative gate biases. Moreover, movement of the ions within the oxide can cause the drain current observed at a given bias point to drift as a function of time. (The threshold voltage changes with time corresponding to the voltage translation of the C–V characteristics in the MOS-C analysis.) If present in large densities the interfacial traps which "spread out" the MOS-C C–V characteristics can likewise increase the change in gate voltage required to achieve a desired ΔI_D at a given drain voltage. In other words, interfacial traps can reduce the "gain" ($\Delta I_D/\Delta V_{G|V_D}$) of a transistor. While it is true that both the mobile ion and interfacial trap problems were minimized early in MOSFET development, the remaining nonidealities, primarily through their effect on V_T, have had a large (incredibly large) impact on fabrication technology, device design, and modes of operation. In this section we will examine a number of related items which generally fall under the heading of threshold considerations.

5.3.1 Threshold Voltage Relationships

An expression for the threshold voltage V_T' exhibited by an ideal device is readily established using the delta-depletion formulation and relevant relationships previously presented in Section 3.2. Specifically, combining Eqs. (3.7) to (3.9) and noting $V_G' = V_T'$ when $U_S = 2U_F$, one obtains

$$V_T' = \frac{kT}{q} 2U_F + \frac{q(N_A - N_D)}{K_S \varepsilon_0} x_o' \left[\frac{2K_S \varepsilon_0}{q(N_A - N_D)} \frac{kT}{q} 2U_F \right]^{1/2} \tag{5.27}$$

or

$$V_T' = \begin{cases} 2\phi_F + \dfrac{1}{C_o}\sqrt{4qN_A K_S \varepsilon_0 \phi_F} & \text{for } n\text{-channel } (p\text{-bulk}) \text{ devices} \quad (5.28a) \\ 2\phi_F - \dfrac{1}{C_o}\sqrt{4qN_D K_S \varepsilon_0 (-\phi_F)} & \text{for } p\text{-channel } (n\text{-bulk}) \text{ devices} \quad (5.28b) \end{cases}$$

where, as previously defined, $\phi_F = (kT/q)U_F$.

An expression for the threshold voltage V_T exhibited by a real device is next established by simply evaluating Eq. (4.16) at the $U_S = 2U_F$ point; i.e.,

$$V_T = V_T' + \phi_{MS} - \frac{Q_F}{C_o} - \frac{Q_M \gamma_M}{C_o} - \frac{Q_{IT}(2U_F)}{C_o} \tag{5.29}$$

Moreover, note that evaluating Eq. (4.16) at the Flat Band ($U_s = 0$) point yields

$$V_{FB} = V_{G|U_s=0} = \phi_{MS} - \frac{Q_F}{C_o} - \frac{Q_M \gamma_M}{C_o} - \frac{Q_{IT}(0)}{C_o} \tag{5.30}$$

Thus, if $Q_{IT}(2U_F)/C_o \simeq Q_{IT}(0)/C_o$, a reasonably good approximation in well-made devices, one can also write

$$\boxed{V_T = V_{FB} + V_T'} \tag{5.31}$$

5.3.2 Threshold, Terminology, and Technology

As a lead into the discussion let us perform a simple threshold voltage computation employing relationships developed in the preceding subsection. Suppose the gate material is Al, the Si surface orientation is (111), $T = 23°C$, $x_o = 0.1\ \mu$, $N_A = 10^{15}/cm^3$, $Q_F/q = 2 \times 10^{11}/cm^2$, $Q_M = 0$, and $Q_{IT} = 0$. For the given n-channel device one computes $\phi_{MS} = -0.98$ V, $-Q_F/C_o = -0.93$ V, $V_{FB} = -1.91$ V, $V_T' = 1.00$ V and $V_T = -0.91$ V. Observe: whereas V_T' is positive, as expected, nonidealities of a very realistic magnitude cause V_T to be negative. Since an n-channel device turns-on for gate voltages $V_G > V_T$, the device in question is already "on" at a gate bias of zero volts. Actually, negative biases must be applied to turn the device off! For a p-channel device with identical parameters (except, of course, for an N_D doped substrate) one obtains a $V_T' = -1.00$ V, $V_{FB} = -1.91$ V, and $V_T = -2.91$ V. In the p-channel case the considered nonidealities merely increase the negative voltage required to achieve turn-on.

When a MOSFET is "on" at $V_G = 0$ V, the transistor is referred to as a *depletion mode* device; when a MOSFET is "off" at $V_G = 0$ V, it is called an *enhancement mode* device. Routinely fabricated p-channel MOSFET's constructed in the standard configuration are ideally and practically enhancement mode devices. n-channel MOSFET's are also ideally enhancement mode devices. However, because nonidealities tend to shift the threshold voltage toward negative biases in the manner indicated in our sample calculation, early n-channel MOS transistors were typically of the depletion mode type. Up until ~1977 this difference in behavior led to the total dominance of *PMOS* technology over *NMOS* technology; that is, IC's incorporating p-channel MOSFET's dominated the commercial marketplace. Subsequently, as explained under the heading of threshold adjustment, NMOS, which is to be preferred because of the greater mobility of electrons compared to holes, benefited from technological innovations widely implemented in the late 1970s and is now incorporated in the majority of newly designed IC's.

While on the topic of the threshold voltage in practical devices, it is relevant to note that the inversion threshold of regions adjacent to the device proper is also of concern. Consider, for example, the unmetallized region between the two n-channel MOS transistors pictured in Fig. 5.9(a). If the potential at the unmetallized outer oxide surface is assumed to be zero (normally a fairly reasonable assumption) and if the threshold voltage for the n-channel transistors is negative, then the intermediate region between the two transistors will be inverted. In other words, a conducting path, a pseudo-channel, will exist between the transistors. This undesirable condition was another nuisance in early

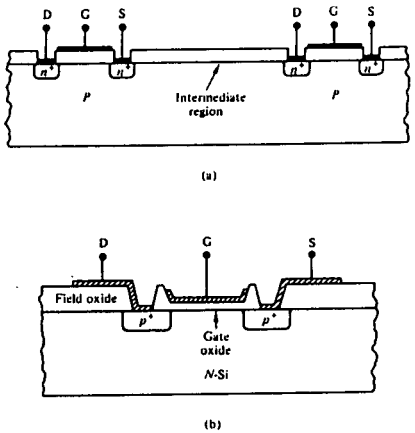

Fig. 5.9 (a) Visualization of the intermediate region between two MOSFET's. (b) Identification of the gate-oxide and field-oxide regions in practical MOSFET structures.

NMOS technology, where, as already noted, nonidealities tended to invert the surface of the semiconductor in the absence of an applied gate bias. Unless special precautions are taken, unwanted pseudo-channels between devices can also arise in both n- and p-channel IC's from the potential applied to the metal overlays supplying the gate and drain biases. To avoid this problem the oxide in the nongated portions of the IC, referred to as the *field-oxide*, is typically much thicker than the *gate-oxide* in the active regions of the structure (see Fig. 5.9(b)). The idea behind the use of the thicker oxide can be understood by referring to Eqs. (5.28) and (5.30). Both V_T' and V_{FB} contain terms which are proportional to $1/C_o = x_o/K_O\varepsilon_o$. Thus employing an x_o (field-oxide) $\gg x_o$ (gate-oxide) increases $|V_T|$ in the field-oxide areas relative to the gated areas in PMOS (and modern NMOS) structures. Inversion of the field-oxide regions is thereby avoided at potentials normally required for IC operation.

5.3.3 Threshold Adjustment

Several physical factors affect the threshold voltage and can therefore be used to vary the V_T actually exhibited by a given MOSFET. We have, in fact, already cited the adjustment of V_T through a variation of the oxide thickness. Obviously, the substrate doping can also

be varied to increase or decrease the threshold voltage. However, although strongly influencing the observed V_T value, the gate-oxide thickness and substrate doping are predetermined in large part by other design restraints.

Other factors that play a significant role in determining V_T are the substrate surface orientation and the material used in forming the MOS gate. As first noted in Section 4.3, the Q_F in MOS devices constructed on (100) surfaces is ~3 times smaller than the Q_F in devices constructed on (111) surfaces. The use of (100) substrates therefore reduces the ΔV_G associated with the fixed oxide charge. The use of a polysilicon instead of an Al gate, on the other hand, makes ϕ_{MS} less negative or even positive. Given a polysilicon gate the effective "metal" workfunction becomes

$$\text{“}\Phi_M\text{”} = \chi_{Si} + (E_c - E_F)_{\text{poly-Si}} \tag{5.32}$$

and

$$\phi_{MS} = \frac{1}{q}[(E_c - E_F)_{\text{poly-Si}} - (E_c - E_F)_{x,\ \text{crystalline-Si}}] \tag{5.33}$$

If we redo the calculation performed in the preceding subsection assuming a typically doped p-type polysilicon gate where $E_F \simeq E_v$, we obtain a $\phi_{MS} = +0.26$ V and $V_{FB} \rightarrow -0.67$ V. If the substrate orientation is also changed from (111) to (100) causing a threefold reduction in Q_F, V_{FB} is further increased to $V_{FB} = -0.05$ V. *Note*: V_T now becomes $V_T = +0.95$ V. Thus positive NMOS thresholds are possible in (100)-oriented structures incorporating polysilicon gates.

Although the foregoing calculation shows positive threshold voltages are possible, actual structures may be only nominally positive. For various reasons a larger threshold voltage may be desired, or one may desire to modify the threshold attainable in a PMOS structure, or tailoring of the threshold for both n- and p-channel devices on the same IC chip may be required. For a number of reasons, it is very desirable to have a flexible threshold adjustment process where V_T can be controlled essentially at will. In modern device processing this is accomplished through the use of *ion implantation*.

The general ion implantation process was described in Section 1.1 of Volume II. To adjust the threshold voltage, a relatively small, precisely controlled number of either boron or phosphorus ions is implanted into the near-surface region of the semiconductor. When the MOS structure is depletion or inversion biased, the implanted dopant adds to the exposed dopant-ion charge near the oxide–semiconductor interface and thereby translates the V_T exhibited by the structure. The implantation of boron causes a positive shift in the threshold voltage; phosphorus implantation causes a negative voltage shift. For shallow implants the procedure may be viewed to first-order as placing an additional "fixed" charge at the oxide–semiconductor interface. If N_I is the number of implanted ions/cm^2 and $Q_I = \pm qN_I$ is the implant-related donor (+) or acceptor (−) charge/cm^2 at the oxide–semiconductor interface, then, by analogy with the fixed charge analysis of Section 4.3 (Volume IV),

$$\Delta V_{G|\text{ions}} = -\frac{Q_I}{C_o} \tag{5.34}$$

Assuming, for example, an $N_I = 5 \times 10^{11}$ boron ions/cm^2 and an $x_o = 0.1\ \mu$, computes a threshold adjustment of +2.32 V.

5.3.4 Back Biasing

Reverse biasing the back contact or bulk of a MOS transistor relative to the sourc another method which has been employed to adjust the threshold potential. This electr method of adjustment, which predates ion implantation, makes use of the so-ca *body effect* or substrate-bias effect.

To explain the effect let us consider the n-channel MOSFET shown in Fig. 5.1C If the back-to-source potential difference (V_{BS}) is zero, inversion occurs of course w the voltage drop across the semiconductor $[(kT/q)U_S]$ equals $2\phi_F$ as picture Fig. 5.10(b). If $V_{BS} < 0$, the semiconductor still attempts to invert when $(kT/q$ reaches $2\phi_F$. However, with $V_{BS} < 0$ any inversion layer carriers which do appear a semiconductor surface migrate laterally into the source and drain because t regions are at a lower potential. Not under $(kT/q)U_S = 2\phi_F - V_{BS}$, as picture Fig. 5.10(c), will the surface invert and normal transistor action begin. In essence, t

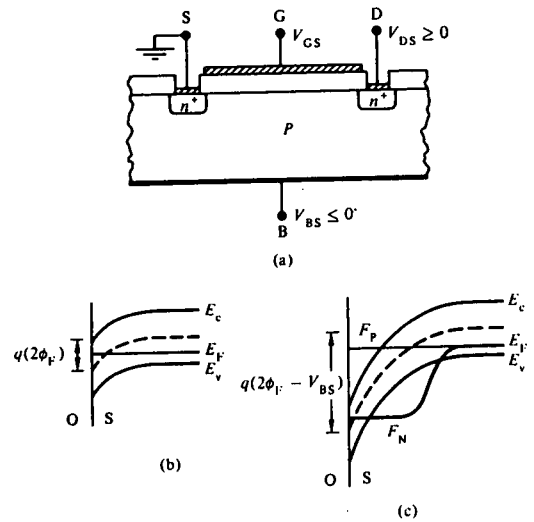

Fig. 5.10 The back-biased MOSFET. (a) Cross-sectional view indicating the double subsc voltage variables used in the analysis. Also shown are the semiconductor energy band dia corresponding to the onset of inversion when (b) $V_{BS} = 0$ and (c) $V_{BS} < 0$.

biasing changes the inversion point in the semiconductor from $2\phi_F$ to $2\phi_F - V_{BS}$. The ideal device threshold potential given by Eq. (5.28a) is in turn modified to

$$V'_{GB|\text{at threshold}} = 2\phi_F - V_{BS} + \frac{1}{C_o}\sqrt{2qN_AK_S\varepsilon_0(2\phi_F - V_{BS})} \quad \text{for } n\text{-channel devices } (V_{BS} < 0) \tag{5.35}$$

Since $V'_{GB|\text{at threshold}} = V'_{GS|\text{at threshold}} - V_{BS}$, we can alternatively write

$$V'_{GS|\text{at threshold}} = \begin{cases} 2\phi_F + \dfrac{1}{C_o}\sqrt{2qN_AK_S\varepsilon_0(2\phi_F - V_{BS})} & \text{for } n\text{-channel devices } (V_{BS} < 0) \quad (5.36a) \\ 2\phi_F - \dfrac{1}{C_o}\sqrt{2qN_DK_S\varepsilon_0(V_{BS} - 2\phi_F)} & \text{for } p\text{-channel devices } (V_{BS} > 0) \quad (5.36b) \end{cases}$$

Having established Eq. (5.36), we make the following observations concerning back biasing or the body effect: (1) Back biasing always increases the magnitude of the ideal device threshold voltage. It therefore makes the p-channel threshold of actual devices more negative and the n-channel threshold more positive — it cannot be used to reduce the negative threshold of a p-channel MOSFET. (2) The current–voltage relationships developed in Section 5.2 are still valid when $V_{BS} \neq 0$ provided $2\phi_F \rightarrow 2\phi_F - V_{BS}$, $V_G \rightarrow V_{GS}$, $V_D \rightarrow V_{DS}$, and V_T is interpreted as $V_{GS|\text{at threshold}}$. (3) Care must be exercised in describing back-biased structures to properly identify voltage differences through the use of double-subscripted voltage variables. The use of double subscripts is, in fact, standard practice in circuit oriented MOS work. However, for convenience and simplicity of notation, the single subscripts (with the back contact assumed to be at ground potential) are routinely employed in works primarily concerned with MOS device physics.

5.4 ac RESPONSE

5.4.1 Small Signal Equivalent Circuits

If one examines the development leading to the low-frequency circuit for the J-FET it becomes immediately obvious that, with very little modification, the Section 1.4 arguments are equally valid for the MOSFET. Without further explanation one can therefore assert that the low-frequency ac response of the MOSFET is characterized by the small signal equivalent circuit displayed in Fig. 5.11(a), where

$$g_d \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=\text{constant}} \quad \text{the drain or channel conductance} \tag{5.37a}$$

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{constant}} \quad \text{transconductance or mutual conductance} \tag{5.37b}$$

Explicit g_d and g_m relationships obtained by direct differentiation of Eqs. (5.13), (5.17), and (5.25) using the Eq. (5.37) definitions are catalogued in Table 5.1.